

FIG. 1

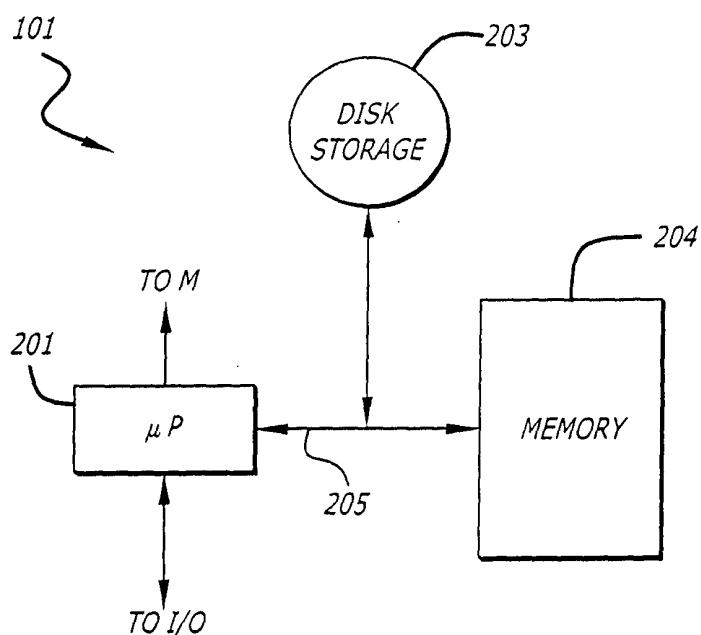


FIG. 2

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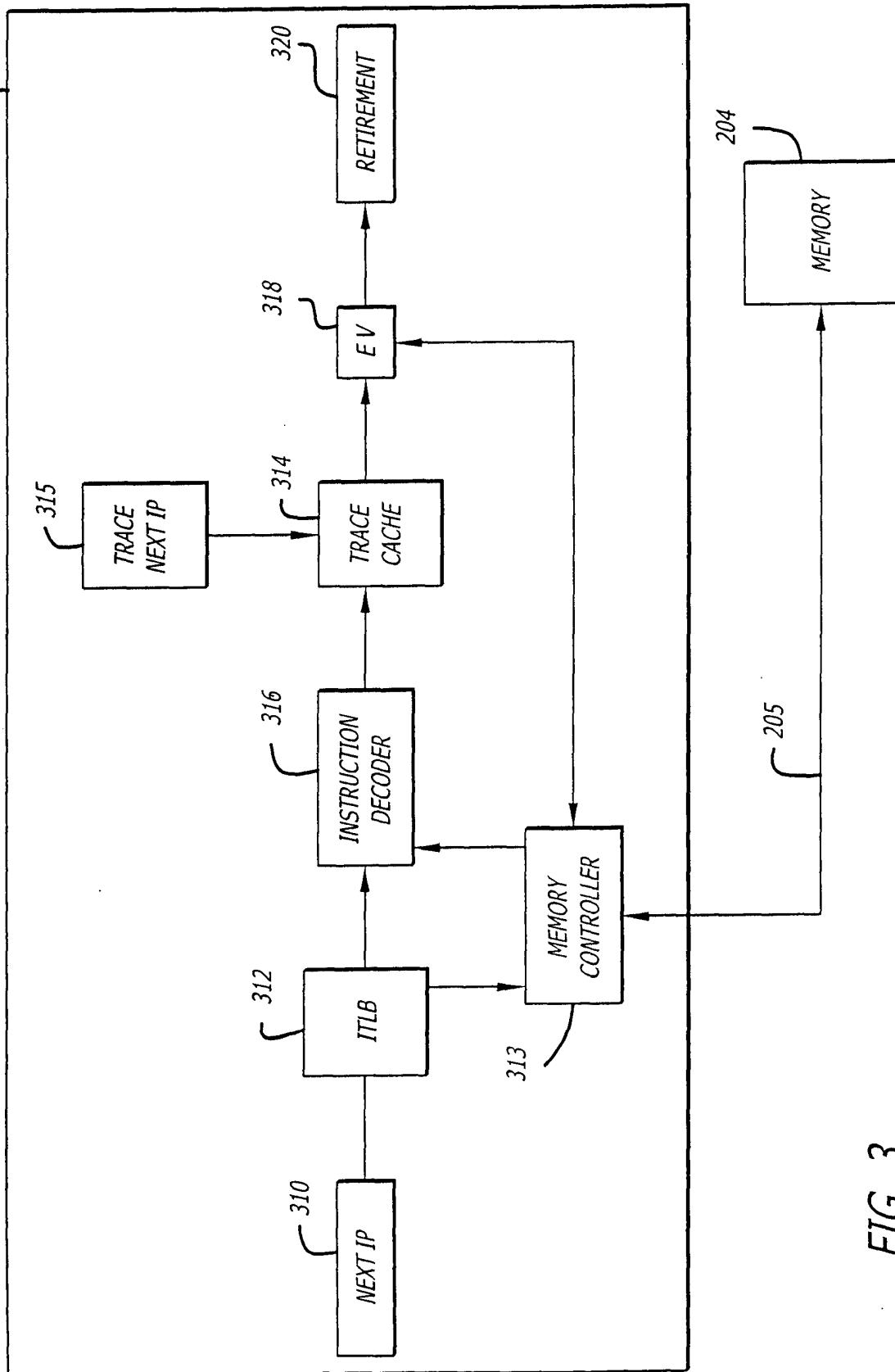


FIG. 3

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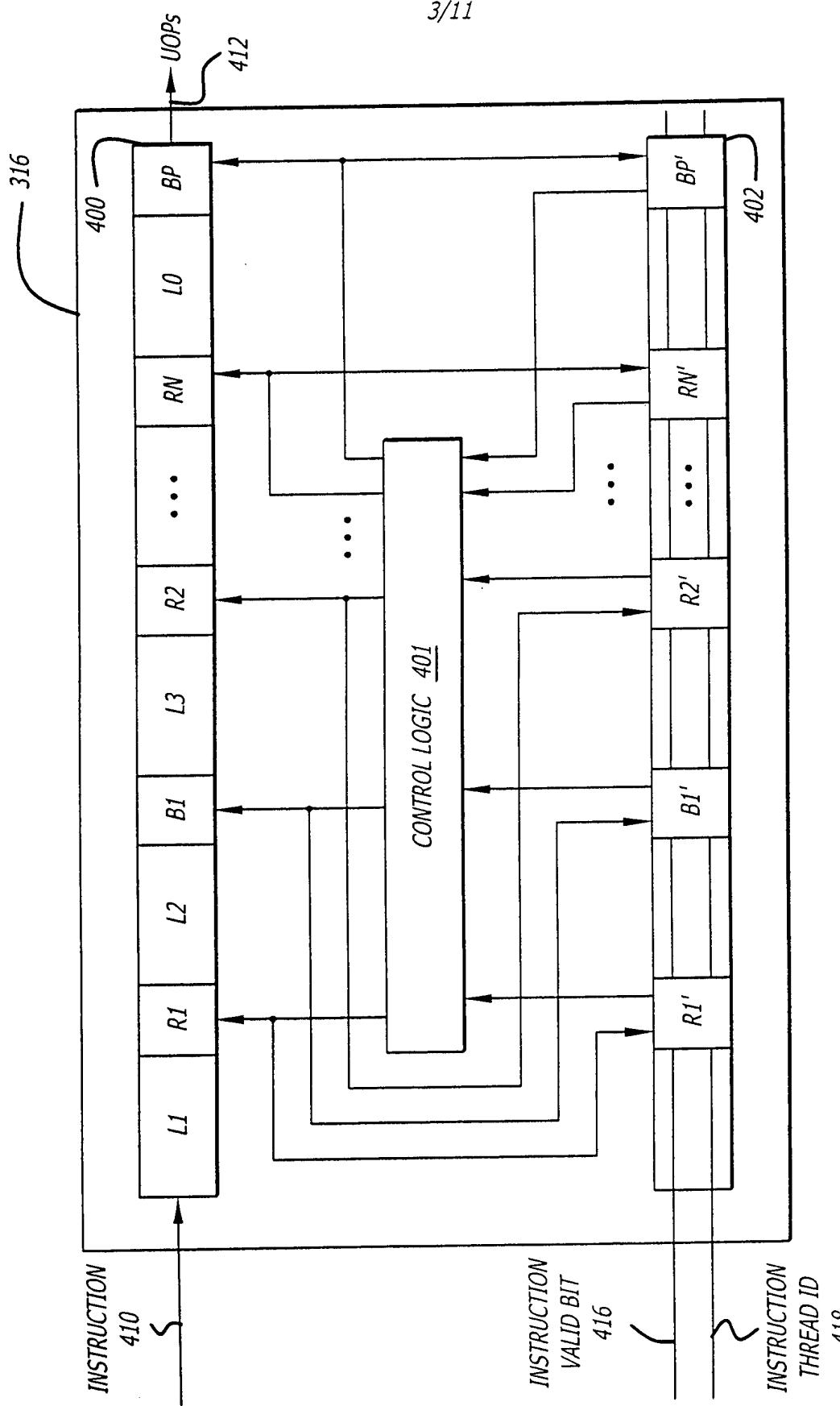


FIG. 4

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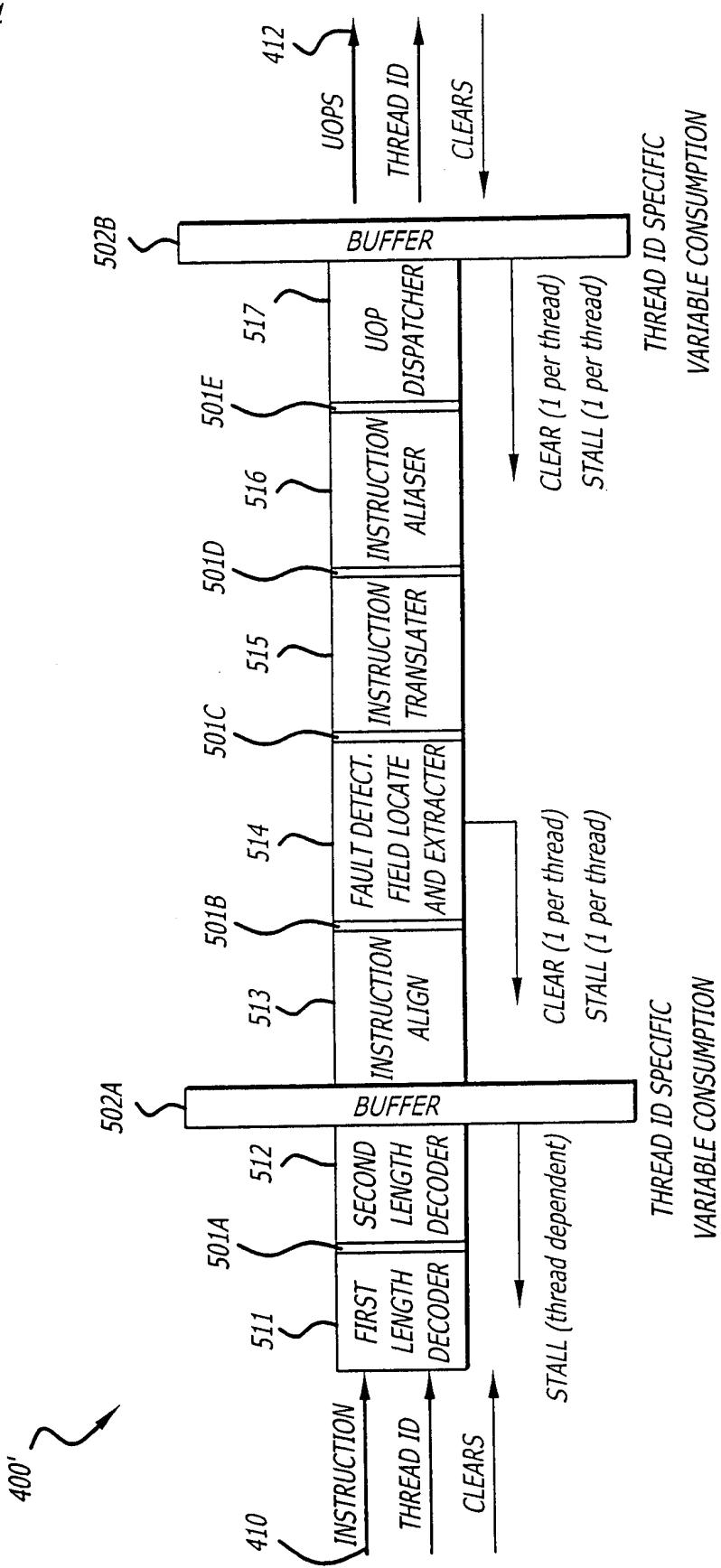


FIG. 5

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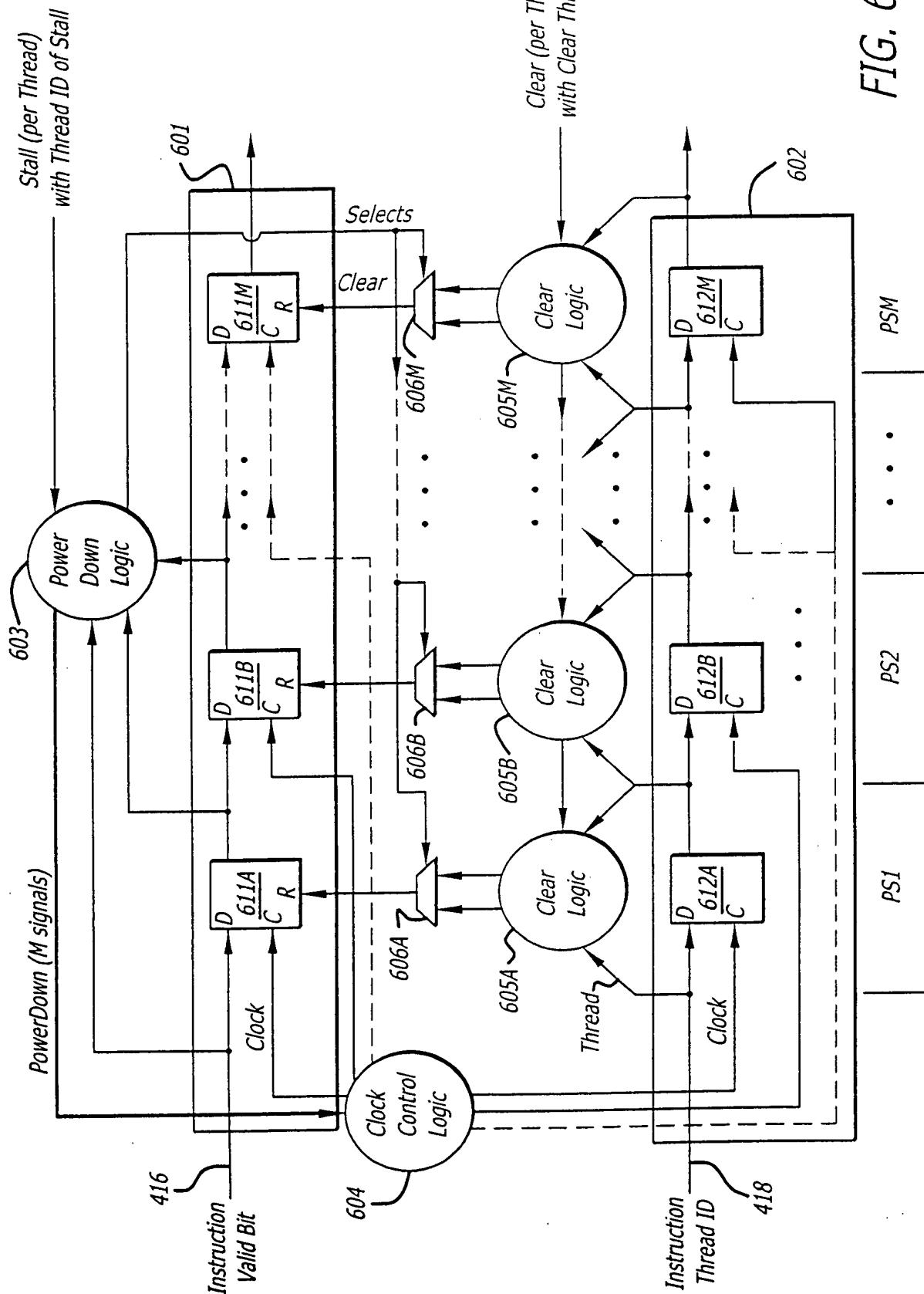


FIG. 6

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Stall for Next to Last PipeStage (NLP)
Stall (NLP) = Valid Instruction in Pipe (NLP) AND (ThreadId (NLP) = ThreadId of Stall)

Stall for any other PipeStageX
Stall(X) = Valid Instruction in Pipe(X) AND Valid Instruction in Pipe(X+1) AND Stall (NLP)

Powerdown for any PipeStage X
Powerdown(X) = NOT Valid Instruction in Pipe(X-1)

Clock Enable for any PipeStage X
Clock(X) = NOT Stall(X) AND NOT Powerdown(X)

Clock for any PipeStage X
Clear (X) = Clock(X) AND [(ClearThread (Id0) AND (ThreadId (X-1) = Id0)) OR (ClearThread (Id1) AND (ThreadId (X-1) = Id1))]
OR
NOT Clock(X) AND [(ClearThread (Id0) AND (ThreadId (X) = Id0)) OR (ClearThread (Id1) AND (ThreadId (X) = Id1))]

ClearThread (Id0) = There was a Clear on Thread Identification 0

ClearThread (Id1) = There was a Clear on Thread Identification 1

Pipe(X) = Any pipestage in the decode

Pipe(X-1) = Pipestage before Pipe(X)

Pipe(X+1) = Pipestage after Pipe(X)

FIG. 7

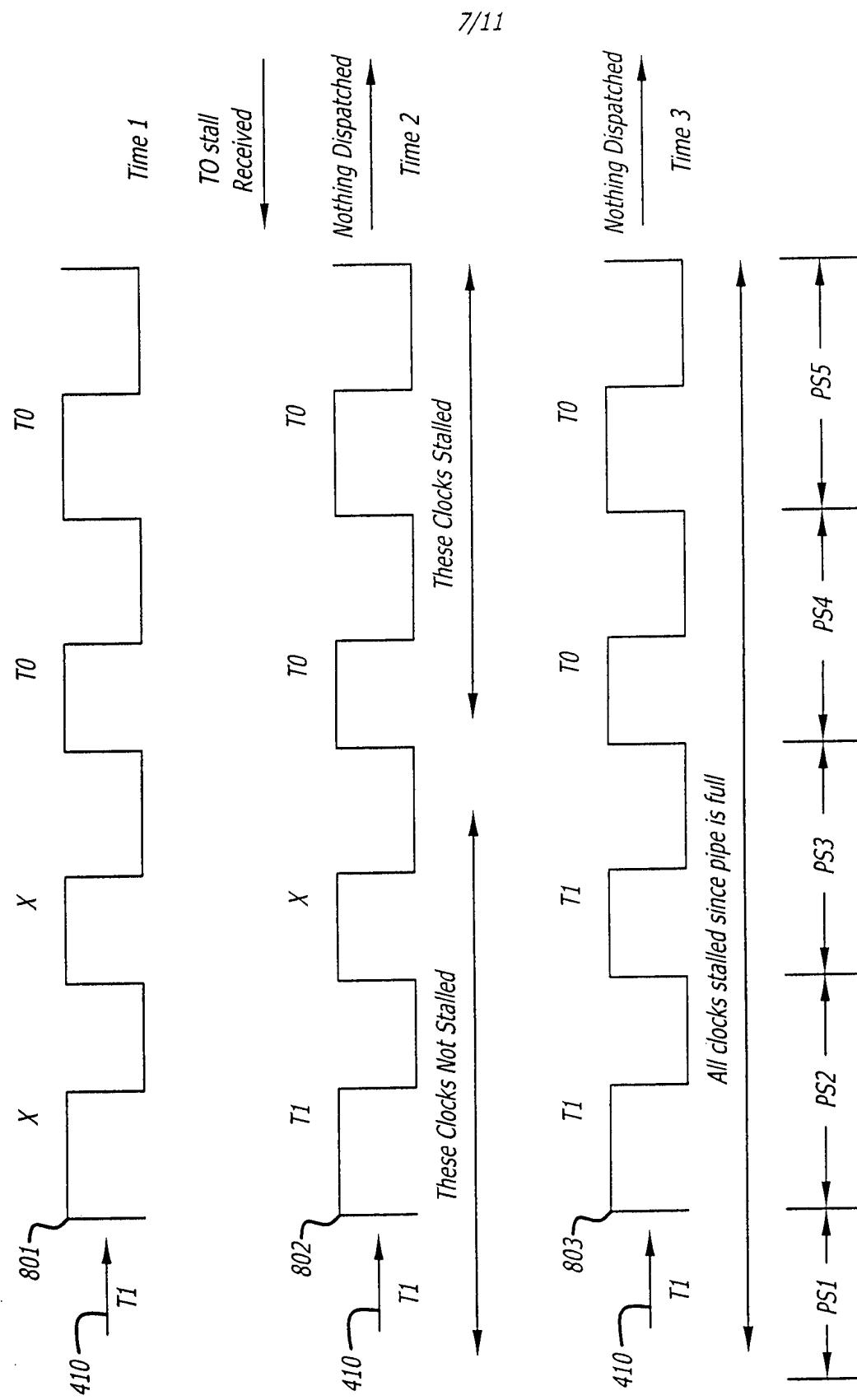


FIG. 8

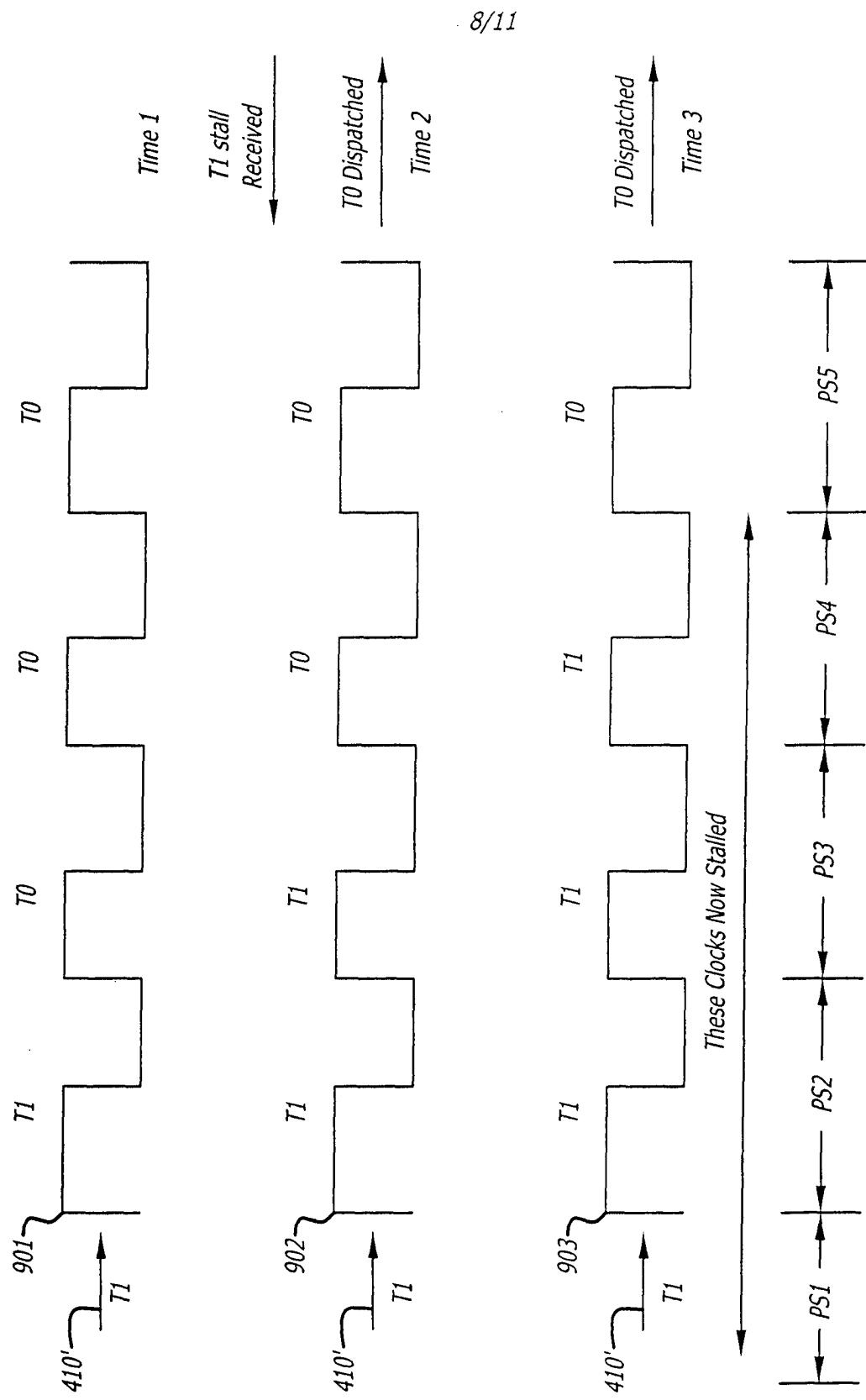


FIG. 9

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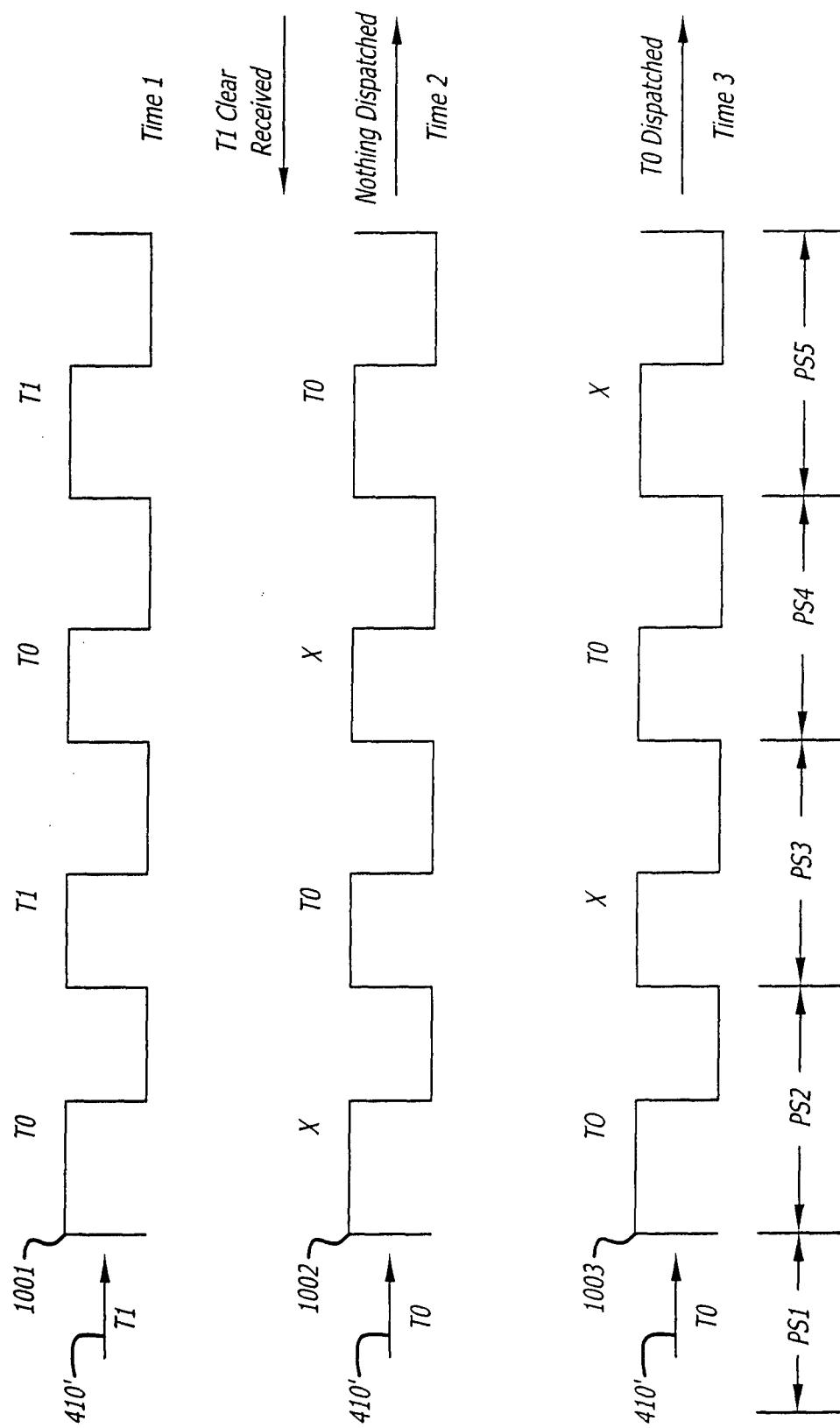


FIG. 10

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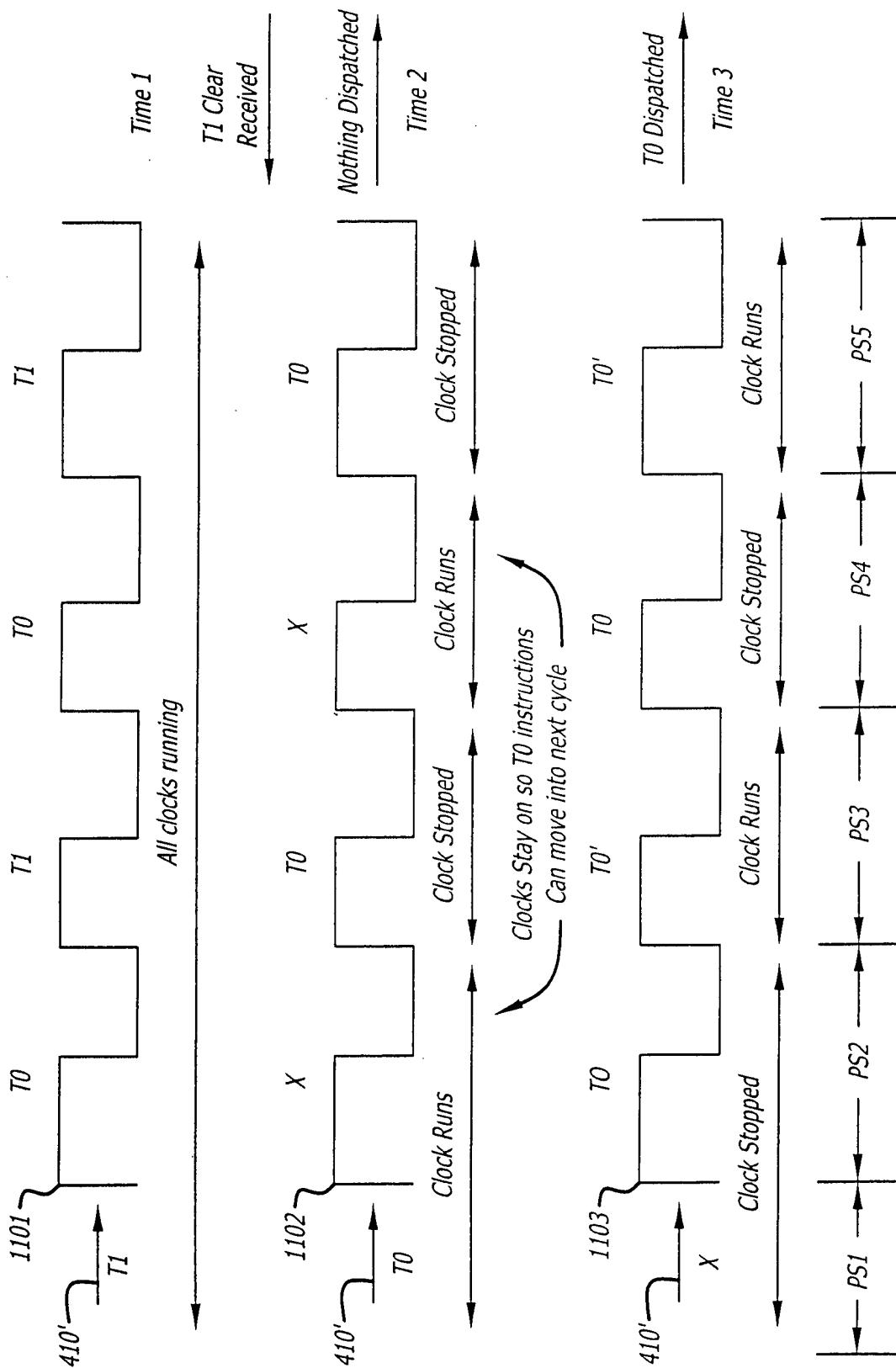


FIG. 11A

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